What is claimed is:

1   1.   An apparatus comprising:

2   a buffer having at least one trigger, coupled with one of a bus and a

3 component connected with said bus, to observe and echo at least one of

4 signals transmitted on said bus, signals transmitted into said component and

5 signals transmitted out of said component;

6   wherein said bus is one of a memory bus, a data bus, an address bus,

7 and a control bus.

1   2.   The apparatus as in claim 1, further comprising an observability port

2 coupled with said buffer to receive said echoed signals, an observability bus

3 connected with said observability port, and a diagnostic device being at least

4 one of a logic analyzer and a bus analyzer connected with said observability

5 bus and performing at least one of detecting said echoed signals, accessing

6 said echoed signals and reading said echoed signals.

1   3.   The apparatus as in claim 2, wherein said observability port is a logic

2 observability port.

1   4.   The apparatus as in claim 1, wherein said bus is one of a simultaneous

2 bi-directional bus (SBD) having ternary logic levels, a single ended bus, a

3 differential bus, an optically coupled bus, a chipset bus, a frontside bus, an

4 input/output (I/O) bus, a peripheral component interconnect (PCI) bus, and an

5 industry standard architecture (ISA) expansion bus.

1   5.   The apparatus as in claim 1, wherein said buffer configured to observe

2 and echo signals transmitted by wireless communication.

1   6.   A method comprising:

2   observing and echoing at least one of signals transmitted on a bus,

3 signals transmitted into a component and signals transmitted out of said

4 component;

5   wherein said bus is one of a memory bus, a data bus, an address bus,

6   and a control bus.

1   7.   The method as in claim 6, further comprising:

2   receiving said echoed signals; and

3   performing at least one of detecting said echoed signals, accessing said

4   echoed signals and reading said echoed signals.

1   8.   The method as in claim 6, wherein said bus is one of a simultaneous bi-

2   directional bus (SBD) having ternary logic levels, a single ended bus, a

3   differential bus, an optically coupled bus, a chipset bus, a frontside bus, an

4   input/output (I/O) bus, a peripheral component interconnect (PCI) bus, and an

5   industry standard architecture (ISA) expansion bus.

1   9.   The method as in claim 6, wherein said signals are transmitted by

2   wireless communication.

1   10.   A system comprising:

2   a memory;

3   an input/output (I/O) port; and

4   a microprocessor;

5   wherein said memory, said I/O port, and said microprocessor are

6   connected by a data bus, an address bus and a control bus; and

7   wherein said microprocessor includes means for observing and echoing

8   at least one of signals transmitted on a bus, signals transmitted into a

9   component and signals transmitted out of said component.

1   11.   The system as in claim 10, further comprising means for receiving said

2   echoed signals, and means for performing at least one of detecting said

3   echoed signals, accessing said echoed signals and reading said echoed

4   signals.

1   12.   The system as in claim 10, wherein said bus is one of a simultaneous bi-

2   directional bus (SBD) having ternary logic levels, a single ended bus, a

3   differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O

4   bus, a peripheral component interconnect (PCI) bus, and an industry standard

5   architecture (ISA) expansion bus.

1   13.   The system as in claim 10, wherein said signals are transmitted by

2   wireless communication.

1   14.   A system comprising:

2   a memory;

3   an input/output (I/O) port; and

4   a microprocessor;

5   wherein said memory, said I/O port, and said microprocessor are

6   connected by a data bus, an address bus and a control bus; and

7   wherein said microprocessor includes a buffer having at least one

8   trigger, coupled with one of said busses and a component connected with said

9   busses, to observe and echo at least one of signals transmitted on said bus,

10   signals transmitted into said component and signals transmitted out of said

11   component.

1   15.   The system as in claim 14, further comprising an observability port

2   coupled with said buffer to receive said echoed signals, an observability bus

3   connected with said observability port, and a diagnostic device being at least

4   one of a logic analyzer and a bus analyzer connected with said observability

5   bus and performing at least one of detecting said echoed signals, accessing

6   said echoed signals and reading said echoed signals.

1   16.   The system as in claim 15, wherein said observability port is a logic

2   observability port.

1   17.   The system as in claim 14, wherein said bus is one of a simultaneous bi-

2   directional bus (SBD) having ternary logic levels, a single ended bus, a

3   differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O

4   bus, a peripheral component interconnect (PCI) bus, and an industry standard

5   architecture (ISA) expansion bus.

1   18.   The system as in claim 14, wherein said buffer is configured to observe

2   and echo signals transmitted by wireless communication.